Module wise Question Bank

SUB (CODE): DDCO(BCS302) **Batch:** 2022
Academic year : 2023-24 (ODD Sem) **Sem:** 3

MODULE 1

1. Define canonical Minterm form and canonical Maxterm form.
2. Express the function F=x+yz as the sum of its minterms and product of maxterms
3. Find the minimal SOP and minimal POS of the following Boolean function using K-Map.
   $f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$
4. With an example explain duality?
5. List all Postulates and Theorems available in Boolean algebra?
6. State and Prove Absorption Theorem.
7. Find the complement and simplify the Boolean function and also write logic circuit
   $F = A'B'C' + A'BC$.
8. Draw a two-level logic diagram to implement the Boolean function
   $F = BC' + AB + ACD$.
9. Implement the Boolean function $F = yz + z'y' + x'z$ With NAND gates.
10. Simplify the following using K-Map technique and find the Essential Prime Implicants.

(*i*) $P = f(w,x,y,z) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$

(*ii*) $Y = f(a,b,c,d) = \sum(0,1,2,6,7,9,10,12) + d(3,5)$. Verify the result using K-map.

(*iii*) $f(A,B,C,D) = \sum m(0,1,2,3,10,11,12,13,14,15)$

(*iv*) $f(W,X,Y,Z) = \sum m(1,3,6,7,8,9,10,12,13,14)$

11. Simplify the following expressions using Karnaugh map. Implement the simplified circuit using the gates as indicated: .

(*i*) $f(w,x,y,z) = \sum m(1,5,7,9,10,13,15) + d(8,11,14)$ using NAND gates.

(ii) $f(A,B,C,D) = \Pi M(0,1,2,4,5,6,8,9,12,13,14)$ using NOR gates.

Proof of all theorems (Very Important)

Simplify the expressions using Karnaugh map. Implement the simplified circuit using the gates(Problems Very Important)

Don't care conditions (Very Important)

MODULE 2

1. What is a multiplexer? Design a 4 to 1 multiplexer using logic gates. Write the truth table and explain its working principle.
2. Construct 4:1 multiplexer using only 2:1 multiplexer(Very Important)
3. Construct 8:1 multiplexer using only 2:1 multiplexer. (Very Important)
4. Design 32 to 1 multiplexer using 16 to 1 multiplexer and one 2 to 1 multiplexer. (Very Important)
5. Mention the differences between decoder and demultiplexer.
6. (a) Realize $Y = A'B + B'C' + ABC$ using an 8 to 1 Multiplexer.(b) Can it be realized with a 4 to 1 multiplexer?
7. Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with the next priority encoding to 11, while the LSB with least priority encoding to 01.
8. Give state transition diagram of SR, D, JK and T flip flops.
9. Obtain the characteristic equation of SR, JK, D and T flip flops.
10. Explain the operation of edge triggered 'SR' flip flop with the help of a logic diagram and truth table. Also draw the relevant waveforms.
11. Explain the working of Master Slave J K flip flops with logic diagram.
12. Derive the Excitation table for equation for D, T,SR, and JK Flip flops.
13. Write Verilog program for demultiplexer.
14. Write Verilog code for 4 bit paralleladder using full adder as component.
15. Differentiate between Latch and flip flop. (Very Important)
16. Differentiate between Combiational Circuit and Sequential Circuit. (Very Important)
17. SR, D, JK and T flip flops.Diagram, Working, Excitation table,Truth table
18. SR Latch circuit diagram anad working(NAND and NOR Gates), Gated SR latches circuit diagram and working, D Latch and (Very Important)
19. Binary Adder- Subtractor, . (Very Important)
20. All lab programs (Very Important)

MODULE 3

1. With a neat diagram explain the different processor registers.

2. What are the factors that affect the performance? Explain any 4.

3. What is performance measurement? Explain the overall SPEC rating for a computer in a program suite.

4. A program contains 1000 instructions. Out of that 25% instructions requires 4 clock cycles, 40% instructions requires 5 clock cycles and remaining requires 3 clock cycles for execution.Find the total time required to execute the program running in a 1GHz machine. (Very Important)

5. Write a note on byte addressability, big-endian and little-endian assignment. (Very Important)

6 Explain the basic operational concepts b/w the processor and the memory. (Very Important)

7.Write down the performance equation? Discuss the measures to improve the performance.

8.Explain processor clock and clock rate.

9.What is an addressing mode? Explain any four addressing modes.(Very Important)

10.Explain functional units of computer. . (Very Important)

11.Discuss connection between processor and memory . (Very Important)

12How input and output operation performed by Processor? (Very Important)

13Explain Bus structure with suitable diagram(Very Important)

14 Explain memory operations in detail. (Very Important)

MODULE 4

1. Define bus arbitration.Explain in detail both approach of bus arbitration. (Very Important)
2. What is an interrupt? With example illustrate the concept of interrupts (Very Important)
3. Explain in detail the situation where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems?
4. Explain the following terms a) interrupt service routine b) interrupt latency c) interrupt disabling.
5. Draw the arrangement of a single bus structure and brief about memory mapped I/O.
6. Explain interrupt enabling,interrupt disabling with respect to interrupts
7. Draw the arrangement for bus arbitrations using a daisychain and explain in brief. (Very Important)
8. With neat sketches explain various methods for handling multiple interrupt requests. (Very Important)

9. Explain memory mapped I/0 and I/0 mapped I/0(Very Important)

10. Compare Memory mapped I/o and I/O mapped I/O(Very Important)

11. Explain how interrupt request from several I/0 devices can be communicated to a processorthrough a single INTR line.

(Very Important)

12What are the different methods of DMA. Explain in brief. (Very Important)

13. Show with diagram the memory hierarchy with respect to speed , size and cost

14. Explain different mapping functions used in cache memory. (Very Important)

. With neat sketches, explain various methods for handling multiple Interrupts requests raised by Multiple devices. **(10 Marks)**

. What is DMA Bus Arbitration? Briefly explain different bus arbitration techniques. **(10 Marks)**

(Very important)

MODULE 5

1.Explain the role of cache memory in pipelining.

2.Explain pipelining performance. (Very Important)

3.Explain the basic concepts of pipelining (Very Important)

4. Explain the single bus organization of the data path inside a processor with suitable diagram. (Very Important)

5. Explain briefly about transferring of contents between registers. (Very Important)
6.Explain the steps involved in Performing ALU operations (Very Important)
7.Explain fetching a word from Memory, Storing a word in memory. . (Very Important)